Notice of Allowability	Application No.	Applicant(s)	
	09/970,766	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	Shouxiang Hu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the 8/23/04 amendment*.

2. ☒ The allowed claim(s) is/are *1-3,9 and 17*.

3. ☒ The drawings filed on *01 July 2003* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *20040911* .
7. ☐ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

SHOUXIANG HU
PRIMARY EXAMINER

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Leana Levin (RN: 51,939) on September 10, 2004.

The application has been amended as follows:

IN THE CLAIMS

1. (Currently Amended) A method of manufacturing a semiconductor substrate comprising the processes of:

forming an insulation film on at least a surface of a semiconductor substrate main body;

forming an ion shield member having a predetermined shape on said insulation film;

subsequent to forming the insulation film, implanting ions into said semiconductor substrate main body from a side on which said insulation film is formed, to thereby form an ion implantation layer;

removing said ion shield member;

cleaning or smoothing the surface of said insulation film;

laminating said insulation film and a support substrate onto each other; and

separating a portion of said semiconductor substrate main body from said support substrate ~~at a portion of~~ along said ion implantation layer,

wherein a shape of an outer edge of said ion shield member is tapered, and thereby said ion implantation layer is partly inclined in response to said tapered shape of the outer edge of said ion shield member, so as to prevent separation defect in remaining portion of the semiconductor substrate main body ~~of~~ on said support substrate.

2. (Currently Amended) A method of manufacturing a semiconductor substrate according to claim 1, wherein the process of separating said portion of said semiconductor substrate main body ~~at the portion of~~ along said ion implantation layer comprises the process of separating said portion of said semiconductor substrate main body at a peak position of an ion concentration in said ion implantation layer.

3. (Currently Amended) A method of manufacturing a semiconductor substrate according to claim 1, wherein the process of forming said ion shield member comprises the processes of: forming an ion shield film made of a resist or an oxide film on said insulation film; and patterning said ion shield film to a predetermined shape to thereby form said ion shield member.

4-8. (Canceled).

9. (Original) A method of manufacturing a semiconductor substrate according to claim 1, wherein a thermally conductive film is buried in the support substrate used in the laminating process.

10-16. (Canceled).

17. (Currently Amended) A method of manufacturing a semiconductor substrate for an electro-optical apparatus, comprising the processes of:

forming an insulation film on a surface of a semiconductor substrate main body;

forming an ion shield member having a predetermined shape on said insulation film;

subsequent to forming the insulation film, implanting ions into said semiconductor substrate main body from a side on which said insulation film is formed, to thereby form an ion implantation layer;

removing said ion shield member;

cleaning or smoothing the surface of said insulation film;

laminating said insulation film and a support substrate onto each other; and

separating a portion of said semiconductor substrate main body from said support substrate ~~at a portion of~~ along said ion implantation layer in a condition that a thickness of a first remaining portion of the semiconductor substrate main body that is designed to form a drive circuit of the electro-optical apparatus is thick and a thickness

of a second remaining portion of the semiconductor substrate main body that is designed to form an image display region of the electro-optical apparatus is ~~thin~~ thinner,

wherein a shape of an outer edge of said ion shield member is tapered, and thereby said ion implantation layer is partly inclined in response to said tapered shape of the outer edge of said ion shield member, so as to prevent separation defect in the first and second remaining portions of said semiconductor substrate main body ~~or~~ on said support substrate.

18. (Canceled).

Allowable Subject Matter

Claims 1-3, 9 and 17 are allowed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is 571-272-1654. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SH
September 11, 2004

SHOUXIANG HU
PRIMARY EXAMINER